Simulation Environment for Investigation Delay Insensitivity of Data Flow Structure Asynchronous Networks and Systems

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Abstract

Clocking is one of the most significant problems of VLSI system design. It is not easy to give a general definition for delay insensitivity, but it is more difficult to verify it for a given digital system. The simulation method proposed by the authors makes possible to follow the classical bottom-up design method from switch level to register-transfer level.
The first step of the proposed designing process is to define a structure consisting of delta-delay DI components in VHDL. The following step of the design process is inserting pulse controlled sample-and-hold type switches into the delta delay architecture. These components are virtual, physically not realised models, and they are referred shortly as TBs (Tansfer Boxes) in the paper. If all gates or cells and their interconnections would be represented by TBs, and all possible sequences including simultaneous activations would be executed, the simulation with positive results can be considered a verification of delay insensitivity. The paper presents the developed special VHDL-FLI simulation environment, the design and simulation process, and shows several interesting problems in which the author's method played an important role.

Keywords: Delay insensitive asynchronous networks, Simulation, VLSI design

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